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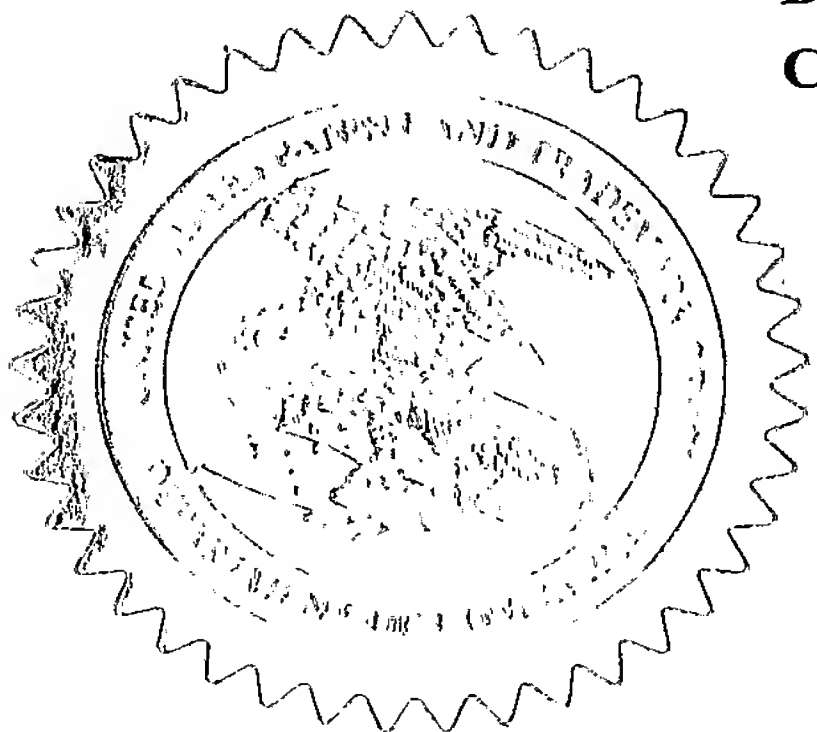**United States Patent and Trademark Office**

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET
This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

INVENTOR(S)

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[ ] Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (280 characters max)

MANAGEMENT OF NETWORK ELECTRONIC COMPONENTS USING NETWORK MANAGEMENT PROTOCOLS

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ENCLOSED APPLICATION PARTS (check all that apply)

[X] Specification   *Number of Pages* | 6 | [ ] CD(s), Number | |

[ ] Drawing(s)   *Number of Sheets* | | [ ] Other (specify) | |

[ ] Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

[X] Applicant claims small entity status. See 37 CFR 1.27.

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[X] The Director is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number | 50-1088 |

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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

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Respectfully submitted,

SIGNATURE _(signature)_   Date | 2/17/2004 |

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REGISTRATION NO. (if appropriate) | 33,613 |

Docket Number: | 71247-0016 |

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

Towards a More Precise Network Management Through Electronic Design

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Abstract

This work proposes an extension of classical network management protocols such as SNMP (Simple Network Management Protocols) for a deep test and management of network electronic components such as routers, switches and PCs. To this end, the proposed approach starts very early in the design process of the integrated circuits that are used in the construction of the managed agents. The approach is based on an extension of design-for-test technique. The approach is described and its efficiency is illustrated through extensive experimentations.

Keywords: Network management, SNMP Protocol, System-on-Chip (SoC), Design-For-Test, P1500 Wrapper.

1. Introduction

Network management becomes mandatory for corporation intranet and extranet. However, there is no mechanism today that allows the management of the electronic components that compose each managed node. Indeed, given a *TCP/IP* network, it is useful to manage not only basic nodes (PCs, routers, terminal servers, ...) but also the electronics, i.e. the integrated circuits which compose such nodes. This can critical for maintenance and on-line testing purposes. This can be made possible if and only if the electronics supports testing and maintenance facilities.

Design-For-Test (*DFT*) techniques consist in integrating testability features at the design stage of electronic components. Such techniques become mandatory for production testing of today integrated circuits and systems. Among the widely used *DFT* techniques there is the *IEEE* standard called *P1500* [1,2,3]. It improves the testability (controllability and observability) of System-on-Chip (*SoC*) by adding more logic. None of these techniques has been considered to facilitate the maintainability and the management of electronic systems (e.g. routers, switches) that belong to a managed *TCP/IP* network. This work shows how to take

benefit from the *P1500 DFT* technique by extending the necessary logic and make is usable by the *SNMP* (Simple Network Management Protocol) management protocol.

A *SoC* which composes a networking device embeds hundreds of million of transistors. Such a huge amount of transistors within a single chip makes possible the implementation of complex functionalities for signal processing, calculation, memorizing, etc.. Designing a *SoC* is mainly based on the use or the reuse of Intellectual Proprieties (*IP*) such as processor *RISC*, *DSP*, *RAM* and *ROM* [4]. Testing is a critical issue in the development and production process of *SoC*.

The proposed approach in this paper enhances the accessibility to *IP Cores*, given a complex *SoC*. It takes advantage of *SNMP* which was originally proposed to enhance the management of *TCP/IP* local area networks, within a SoC for a better testability of all *IP Cores* and consequently of all *SoCs* which constitute the electronis system. Indeed, *P1500* facilitates the access to the internal structure of an *IP Core* and the transfer of the information of test between the provider and the *IP Core* integrator. *SNMP* was originally suggested by the *IETF []*. Known as simple and very efficient, *SNMP* embeds a set of functionalities that allow the management of heterogeneous and complex networks. In this work, *SNMP* is considered beyond the classical framework of network management because it is implemented within a SoC.

An *SNMP*-based network (fig. 1) consists of several components [5,6]: a Network Management Station (*NMS*), a Network element (*NE*), a database called *MIB* (Management Information Base) and the SNMP protocol. The *MIB* is a collection of objects stored into an information virtual base. An *SNMP* agent is a NE. It seeks network information such as the number of erroneous packets and sends them to the NMS.

Main motivations of using *SNMP* as a backbone of a testing strategy are summarized as follows:
- Management and monitoring of the activity of various electronic equipments that are widely used in local networks (computer, router, switch, etc.),
- Collecting of deep state information on the state of each component,
- Detection of network failures,

- Elaboration of a standard management as regards to remote access to information base (*MIB*),
- Take benefit from available network management software tools such as *HPOPENVIEW* of *Hewlett-Packard*.
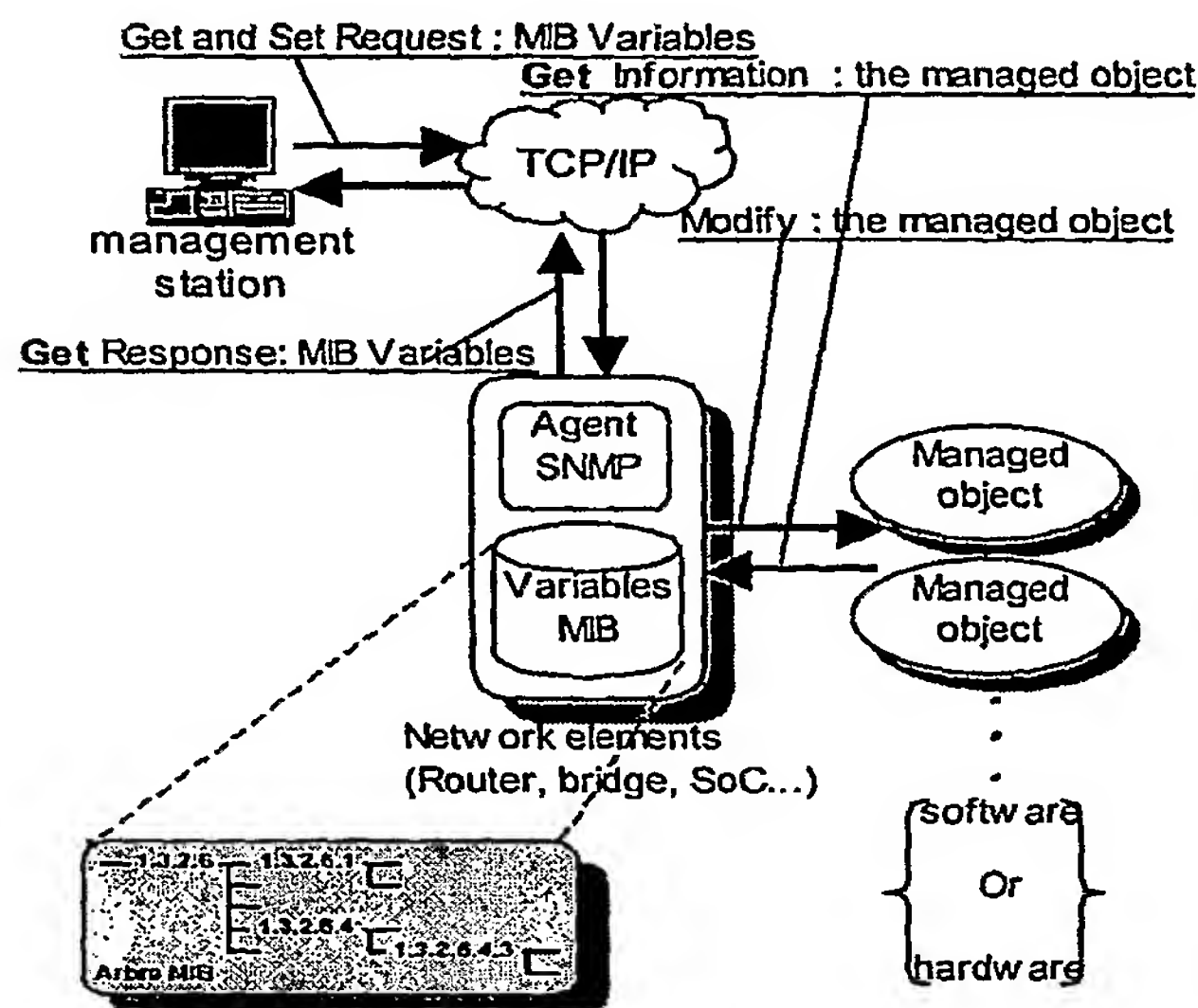

Fig. 1: SNMP environment

More precisely, using the proposed approach, each *IP Core* with a *SoC* behaves as an *SNMP* agent. It is noteworthy that P1500 has been considered for the following reasons: (1) it helps in the isolation of an *IP Core* among those that compose the *SoC*, (2) it provides a standard mechanism of access to internal logic, (3) it facilitates the mix and the interconnection of *IP Cores* which are provided from multiple vendors, (4) it is an *IEEE* standard widely spread and well documented.

This paper is organized as follows. Section 2 presents testing challenges of *SoCs* in the framework of the proposed approach. Section 3 presents the *SNMP* compliant testing architecture. Section 4 describes the details of extended *P1500* architecture. Finally, simulation results are presented before concluding this paper.

2. SoC testing

The new design methodology of SOCs raises new testing problems [1,3,4]. Indeed, testing today integrated circuits involves the responsibility of not only the device manufacturer but also the designer and the *IP Core* provider.

An *IP Core* is tested by the core integrator as a part of a *SoC*. This is accomplished by using test vectors that are given by the *IP Core* provider. Indeed, the integrator of a *SoC* has few information on the used *IP Core*. *IP Cores* are considered as black boxes. Today, more than ever an *IP Core* has to be designed with testability issues in mind [4]: test point insertion, *Scan*, *BIST* insertion, etc.

Hence, the problem of *SoC* testing requires new challenges [1]:

- The transfer of an *IP Core* testing information from the designer to the user,
- The access to a testing *IP Core* infrastructure, so as to be able to reach inputs/outputs and to connect them to an *ATE* (Automatic Test Equipment) or to a *SoC* logic *BIST*.
- The optimization of test integration to ensure a good trade-off *performance/cost*.

Beyond testing, another problem comes from the diversity of the origin and the technology of *IP Cores*. Indeed, the *IP Cores* are heterogeneous from several point of views: the used communication protocols, the used bus interface, frequency, etc. Such heterogeneous parameters imply connection and communication problems between the *IP Cores*. Thus, flexibility and compatibility are more than required by *IP Core* users.

Many test standards have been proposed to make *SoC* testing an easier and less complex problem, in particular the *P1500 IEEE* standard [1,2,3]. Thus, the consortium *VSI (?) alliance* [7] insists on the intensive acceleration of the *SoC* development by specifying standards facilitating the mixture and the interconnection of *IP Core* coming from multiple sources. It also recommends the transfer of the test information between the provider and the integrator.

For test needs, each *IP Core* must be encapsulated in a *P1500 wrapper*. The role of the wrapper is to allow the control of external inputs and to observe external outputs of the *IP Core* by means of a peripheral scan-path. In addition, the wrapper must allow the control of the *IP Core*'s internal scan-path. It also makes possible to define the operating mode of the *IP Core* such as the functional mode/peripheral shift mode/internal shift mode, etc. So that tests information is disseminated within the *SoC* through a test access mechanism (*TAM*: test bus).

An hybrid approach which combines classical DFT and SNMP has several advantages as summarized below:
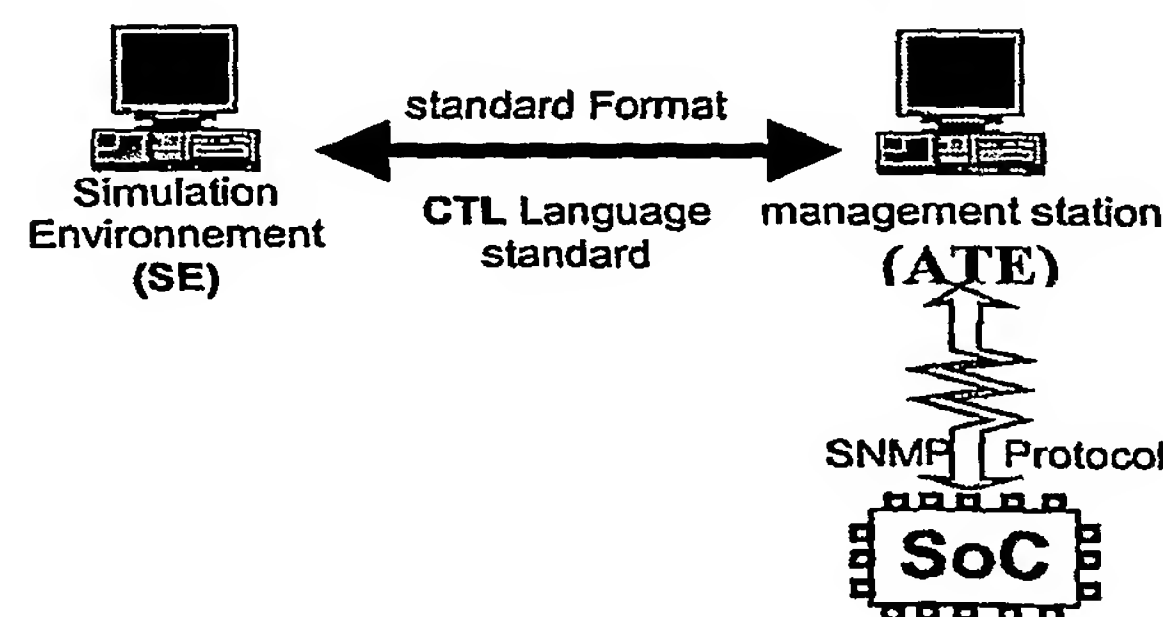

Fig. 2: SoC testing by an ATE

- *Minimization production testing costs:* current testers known as *ATEs* (Automatic Test Equipments) are very expensive. The fact of carrying out test patterns on a remote *SoC* via a *TCP/IP* network (pre-installed) allows using less *ATEs* since each one of them can be used for

several tests. This is made possible since data can be carried out from an *ATE* to an electronic device through a classical *TCP/IP* network technology (see Figure 2).

- *Improving fault diagnosis*: the access to test information (*MIB*) for each individual *IP Core* helps in the diagnosis of a *SoC* internal state. This is ensured through *SNMP* basic instructors such as *SetRequest*, *GetRequest*, *GetNextRequest*, *GetBulkRequest and GetResponse []* .
- *Better maintainability*: using the proposed *DFT* approach makes possible the supervision of the activity of different SoC's *IP*. This allows taking advantage from the important asset in management network domain. Hence, the overall system maintainability is improved.

3. Test architecture

At the architecture level, a *SoC* is considered as embedded distributed system within an electronic device/system. The *IP Cores* are *SNMP* agents that are interconnected by the means of a bus or a complex communication network. This infrastructure is managed starting from a network management station (fig. 3).
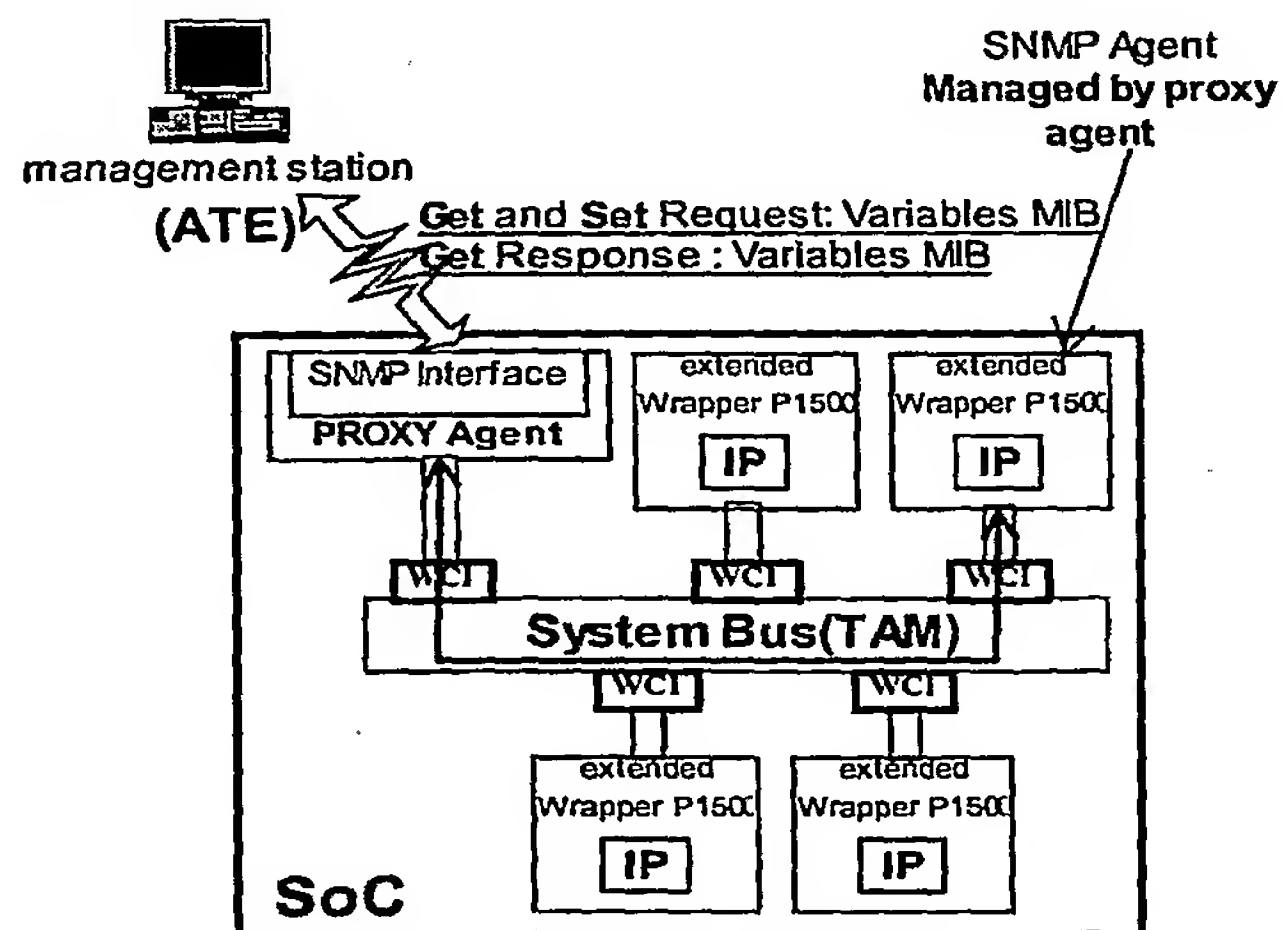

Fig. 3: Test Architecture

The concept of proxy agent is an *SNMP* agent implemented by an embedded micro-controller (fig. 3). It synchronizes the *IP Core* testing. Indeed, it can be considered as an *IP Core* that gets *SNMP* requests (such as *GetRequest, GetNextRequest, GetBulkRequest, SetRequest*, etc.) coming from the station management (or *ATE*: Automatic Equipment Test). These requests are converted towards instructions in conformity with the extended *P1500* standard. Furthermore, the proxy agent analyzes the answers generated by *IP Cores*. Such answers are *SNMP* requests (*GetResponse or Trap*). Finally, test results are sent to the *ATE* as *SNMP* requests. It is noteworthy that the *MIB* of a proxy agent contains all test results that are

related to a *SoC*. Consequently, each *IP Core* stores a *MIB* that represents the behavior of the *core*.

4. Extended wrapper P1500

Figure 4 shows the structure of the *MIB*. A *MIB* describes the functionalities of the test techniques associated with *P1500* Wrapper as well as information relating to the testing process (e.g. test vectors, test results) within an *IP / SoC*.

This *MIB* is divided in two parts of information: the *SoC* level information and the *IP Cores* level information. The first part is dedicated mainly to the *SoC* level information such as the *SoC* identifier, the cartography information, etc... The second part is dedicated only to *IP Cores* information tests. In this part, we find the information related to *P1500* test architecture for each *IP Cores* regrouped in the table called *"IPCoresWrappedP1500Table"*. The index of this table is *"IPCoreIndex"* that represents the address of *IP Cores* in the *SoC* environment. We can also integrate other test architectures to this *MIB* such as *IEEE 1149.1* standard if the *IP Cores* are wrapped with *IEEE 1149.1* architecture.

4.1 Extended P1500 wrapper Architecture

Figure 5 shows the architecture of the extended wrapper *P1500*. This extension implements a large part of the *MIB* (fig. 4). The architecture of the extended wrapper *P1500* contains the following blocks:
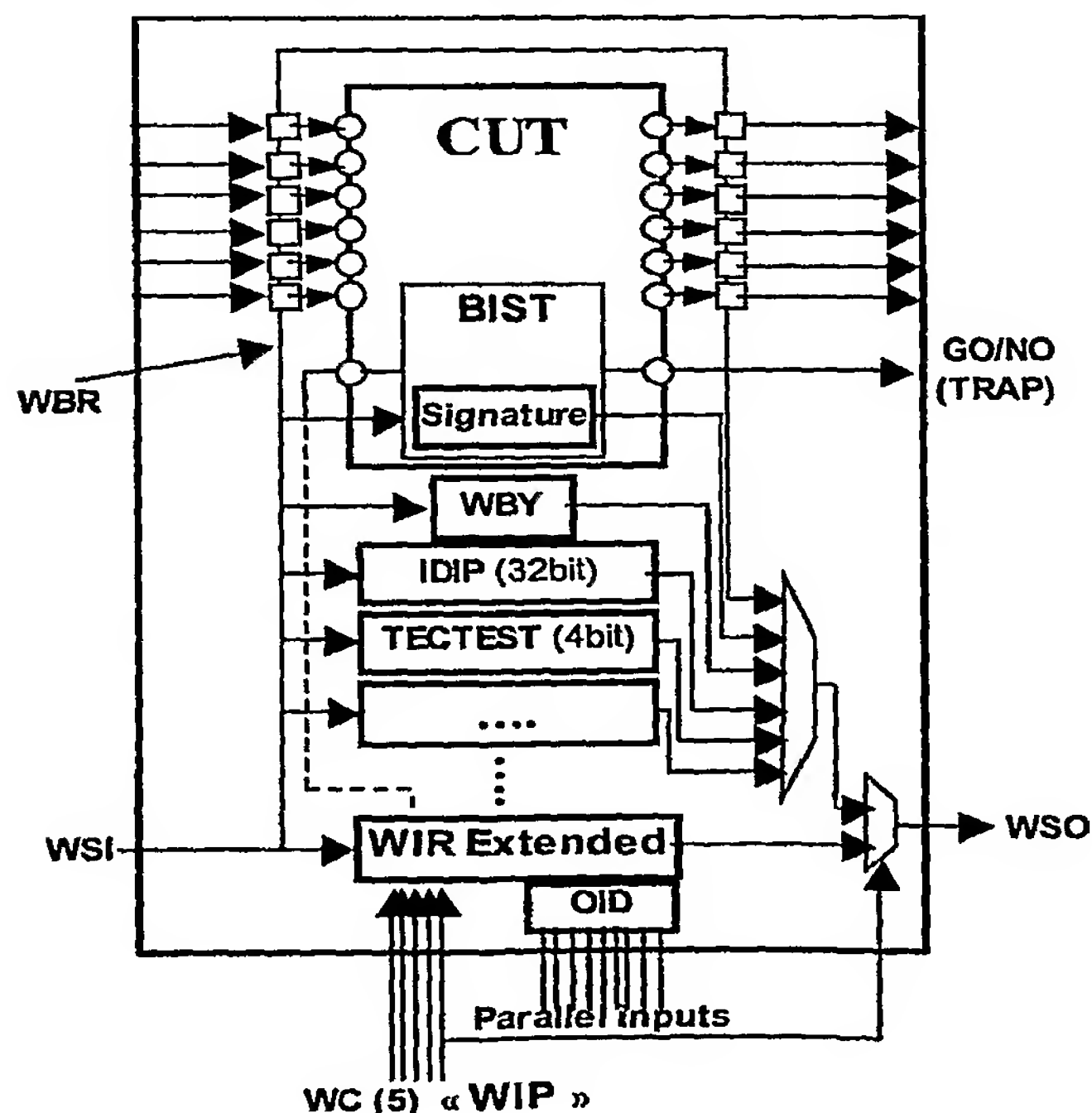

Fig. 5: Extended wrapper P1500

- **IDIP**: a 32 bits register that stores the *IP Core* identifier (i.e.. manufacturer identifier, version, etc.).

- **TECTEST**: a 4 bits register that identifies the used test technique (i.e. scan, BIST...).
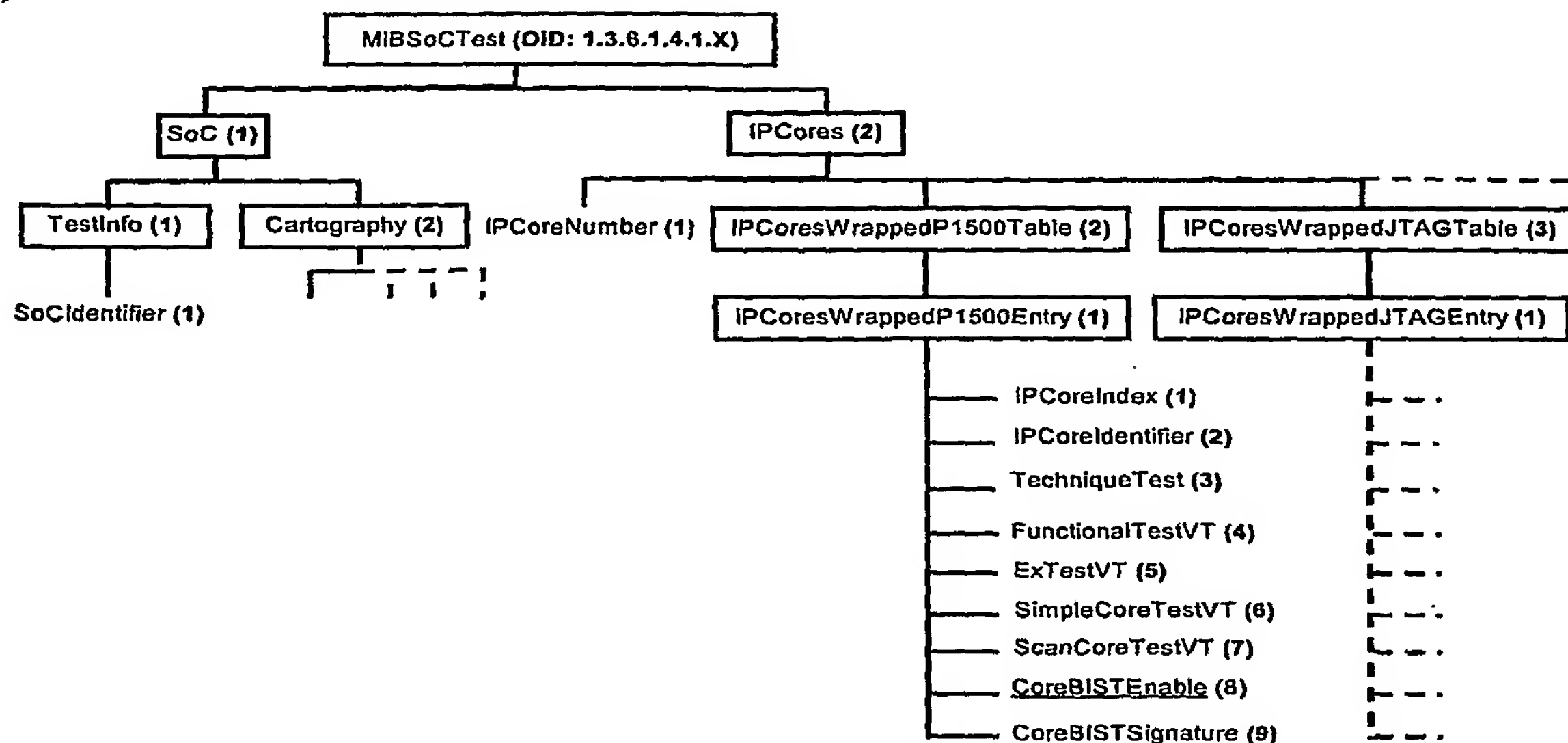

Fig. 4: MIB of test architecture

- **WBY, WBR, WSI, WSO, BIST, WIP**: basic blocks which are already defined by the *P1500* standard [2]. Please refer to [1,2,3,4] for more information.

- **WIR** (Wrapper Instruction Register) **Extended**: this logical block extends the classical *P1500* instruction register in order to support *SNMP* instructions. Indeed, new instructions are necessary for the extended architecture.

- **OID** (Object IDentifier) **register**: this register gets a flatten object identifier from proxy agent. It completes the semantic of the added P1500 instructions.

4.2 SNMP/P1500 relationship

The relationship between SNMP instructions and those of P1500 (see table 3) is implemented as proxy agent level.

At *SoC* level, the control block (proxy agent) converts the *SNMP* requests into *P1500* instructions. For example, the *SNMP* request "**GetRequest X.1.1.1.0**" is converted into **WS_GETREQUEST** *P1500* instruction with flatten Object IDentifier (*OID*) equal **1**. This value of flatten *OID* corresponds to hierarchical *OID* "**X.1.1.1.0**". We use the flatten *OID* inside the *SoC* instead of hierarchical *OID* in order to minimize the logic of treatment of hierarchical *OID* for each *IP Cores*.

Tab. 1: Relationship between instructions

SNMP request	P1500 Instruction
GetRequest X.1.1.1.0	**WS_GETREQUEST** with OID <= 1 ⇔ to recovery of the contents of the register IDSOC which is at proxy agent level.
GetRequest X.2.2.1.2.IPCoreIndex	**WS_GETREQUEST** with OID <= 6 ⇔ recovery of the contents of the register IDIP of IP selected.
SetRequest X.2.2.1.1.1 VT	**WS_SETREQUEST** with OID<=15 ⇔ to start the functional test.
SetRequest X.2.2.1.4.IPCoreIndex VT	**WS_SETREQUEST** with OID<=20 ⇔ to start the external test.
SetRequest X.2.2.1.5.IPCoreIndex VT	**WS_SETREQUEST** with OID<=25 ⇔ to start the internal test.
SetRequest X.2.2.1.6.IPCoreIndex VT	**WS_SETREQUEST** with OID<=30 ⇔ to start the internal test concatenating the WBR with scan chain.
SetRequest X.2.2.1.7.IPCoreIndex VT	**WS_SETREQUEST** with OID<=35 ⇔ to start the integrated test (*BIST*).
GetNextRequest @IP OID	**WS_GETNEXTREQUEST** with the OID: the following *OID* will be calculated starting from the received *OID*.

SNMP/P1500

5. Experimental results

Several experimentations have been carried out using twenty-two benchmarks known as *ITC99 benchmarks[]*. The obtained results are summarized in Figures 5 and 6.
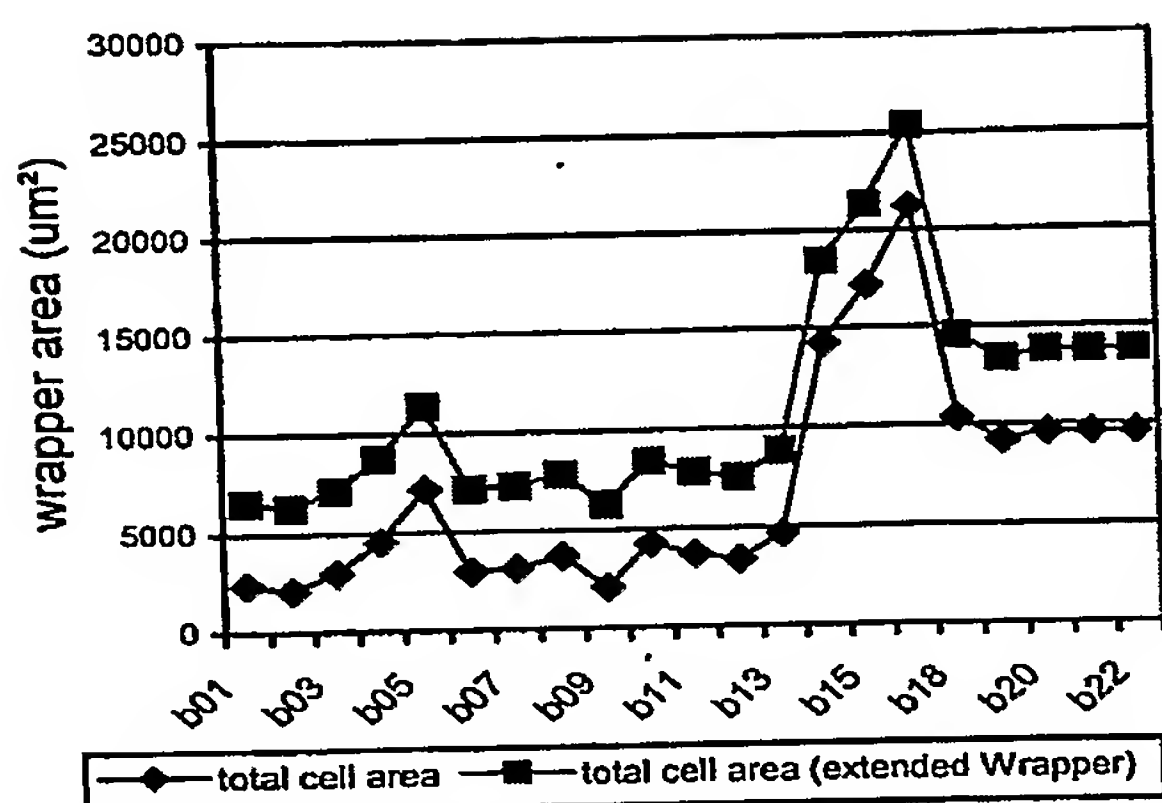
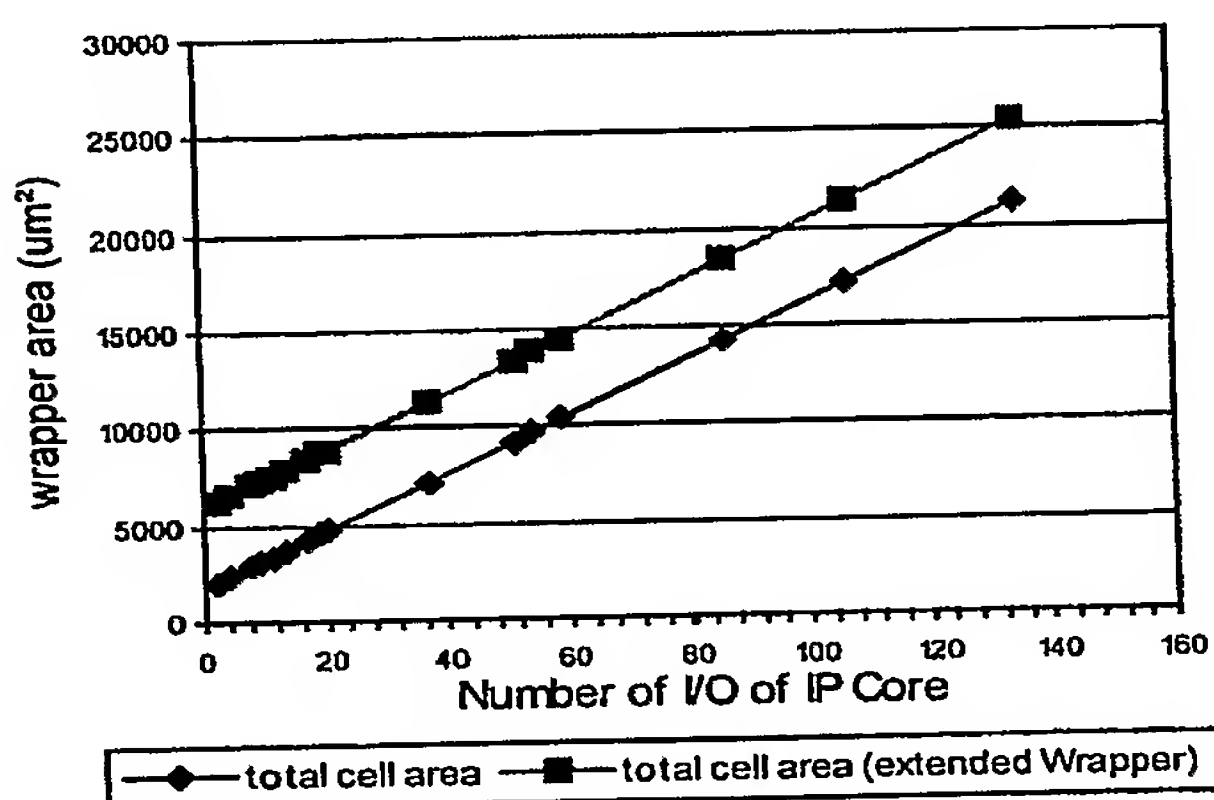Fig. 5: Area Overhead of the extended P1500 interface

Fig. 6: Total area occupied by Wrapper according to the number of input/output of IPs

As show in the above figures, the area is not affected by the proposed architecture. This is also illustrated in Figure 7 which gives the area overhead, the percentage of the area occupied by the extended wrapper compared to the total area of the *IP Core*. Indeed, for a complex *IP Core*, a *SNMP* interface necessitates a few added logic.
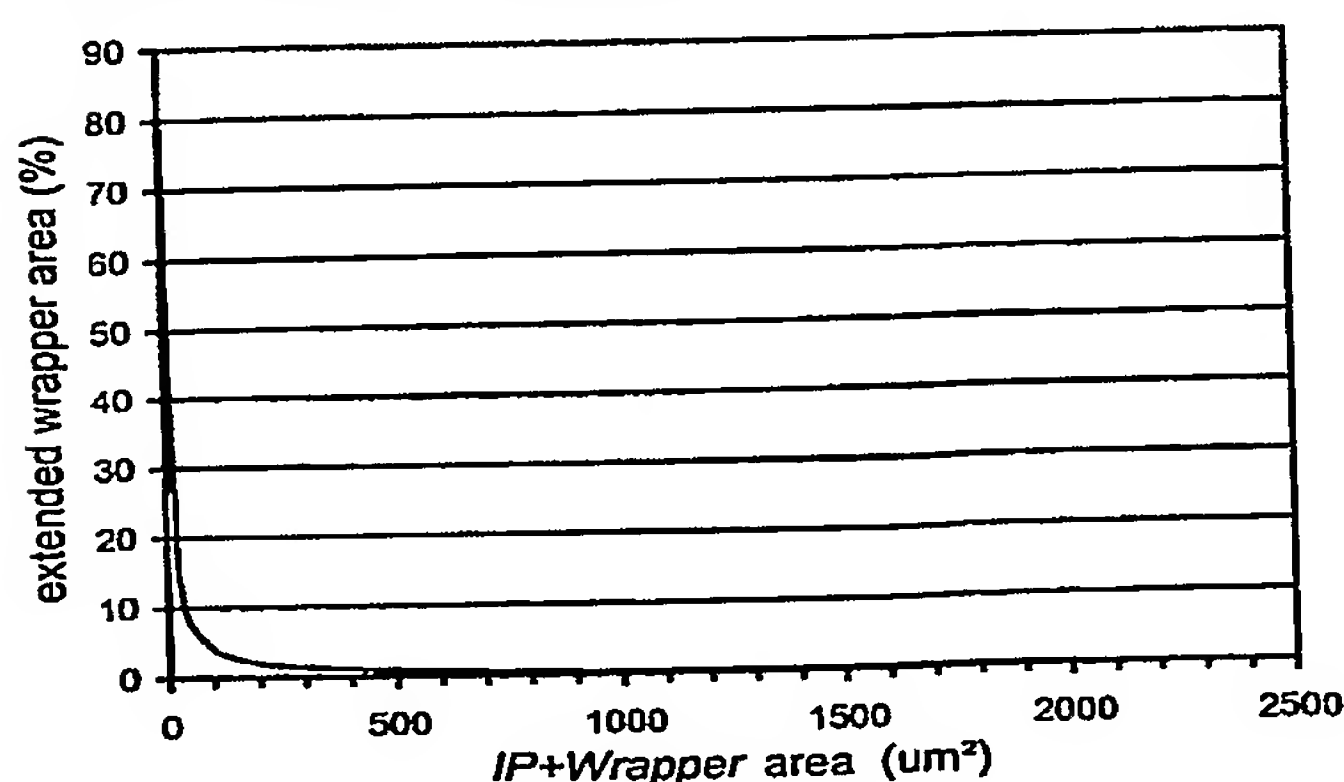

Fig. 7: Area overhead (%) using a SNMP interface

6. Conclusion

In this paper, a new approach that takes advantages of design-for-test of integrated circuits to enhance network management was presented. The approach is based on a combination between a simple network management protocol (*SNMP*) and the *P1500* design-for-test standard. The approach was shown cost-effective on several benchmarks. In future research, the approach will be experimented in a real *TCP/IP* network.

7. References

[1] E. J. Marinissen, R. Kapur and Y. Zorian, "On Using IEEE P1500 SECT for Test Plug-n-Play". *IEEE International Test Conference (ITC)*, pp 770-777, Atlantic City, NJ, October 1-5, 2000.
[2] IEEE P1500 Web Site. http://grouper.ieee.org/groups/1500/
[3] E. J. Marinissen and Y. Zorian, "Challenges in Testing Core –Based System Ics", *IEEE Communication Magazine*, pp 104-109. June 1999.
[4] Y. Zorian, "Embedded Tutorial: System-Chip Test Strategies". *Papers 35th Design Automation Conference ACM*, pp 752, Francisco, USA, June 1998.
[5] M. Rose "gestion des réseaux ouverts SNMPv2" Ed InterEditions, paris 1995
[6] R. Stevens, "TCP/IP illustré volume 1" Ed Vuibert, 1998.
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Complements

La conception des circuits intégrés a beaucoup évoluée depuis quelques années. Les progrès très importants de l'intégration des circuits a permis d'élaborer des circuits qui sont de réels systèmes sur puce (SOC : System on Chip). La conception d'un SoC se base en grande partie sur l'utilisation des propriétés intellectuelles (IP). Un IP correspond à un circuit où un bloc préconçu d'un circuit. L'utilisation des IP dans la conception des SoC permet d'écourter considérablement le temps d'apparition d'un circuit sur le marché (ttm : time-to-market). En revanche, les fournisseurs des IP ne fournissent pas les solutions de test qui l'accompagnent. Par ailleurs, une fois le SoC conçu, aucune solution ne permet de complètement et d'une manière efficace tester le circuit final.

La présente invention vise l'amélioration de testabilité des IP et SoC en se basant sur une technologie « réseaux » TCP/IP sans qu'il faille concidérer ce protocole comme le seul utilisable au sens de l'invention. L'objectif est de rendre accessible à distance un SoC dans son ensemble et/ou un, plusieurs ou tous blocs fonctionnels constituant ledit SoC individuellement.

Une telle possibilité d'accéder aux circuits en utilisant une technologie TCP/IP permet d'effectuer des tests à distance pour un but de partage de ressources coûteuses comme les testeurs de circuits ou ATE (Automatic Test Equipements)

ainsi que d'assurer un test préventif ou de maintenance d'un système électronique complexe.

L' approche de "conception testable" ou "Design-For-Test" au niveau des propriétés intellectuelles et systèmes sur puce permet d'accéder aux information de test (vecteurs de tests, résultats de test) ainsi que d'activer des tests effectifs sur la puce et ceci à travers une technologie réseaux TCP/IP basée sur les protocoles d'administration tels que par exemple mais non exclusivement SNMP (Simple Network Management Protocol).

Il doit être remarqué que cette approche de DFT au niveau des blocs ou IP a été décrite en relation avec la norme P1500 sans qu'il faille considérer que ce soit le seul moyen d'atteindre l'objectif de l'invention .